

**Earth Orbiter-1 (EO-1) Spacecraft  
Wideband Advanced Recorder/Processor  
(WARP) to Atmospheric Corrector (AC)  
Interface Control Document**



EO-1 ICD-057

Baseline

March 11, 1998

National Aeronautics and  
Space Administration

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Goddard Space Flight Center  
Greenbelt, Maryland

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## **Abbreviations and Acronyms**

## Section 1. Overview

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### 1.1 Scope

This interface control document (ICD) defines the interface between the Wide Band Advanced Recorder Processor (WARP) and the Linear Etalon Imaging Spectral Array/Atmospheric Corrector (LEISA/AC or AC).

### 1.2 Supporting Documents

	Computer Networks, 2nd ed., by Andrew Tanenbaum, 1989 (source: GSFC library)
	OSI Explained, by John Henshall and Sandy Shaw, 1988 (source: GSFC library)
AM-149-0020(155)	System Level Electrical Requirements NMP EO-1 Flight, Litton Amecon, 1996
	FUSE Science Data Bus ICD, by Terry Smith, 1993 (source: Terry Smith or Evan Webb)
	EO-1 to LAC ICD
SAI-SPEC-158	EO-1 Verification Plan and Environmental Specification

### 1.3 Requirements

The WARP/AC interface is made up of mechanical and electrical constituents. The mechanical interface consists of a 78-pin connector and associated wiring harness. The electrical interface consists of a 32-bit differential data bus and two differential control signals.

### 1.4 Interface Description

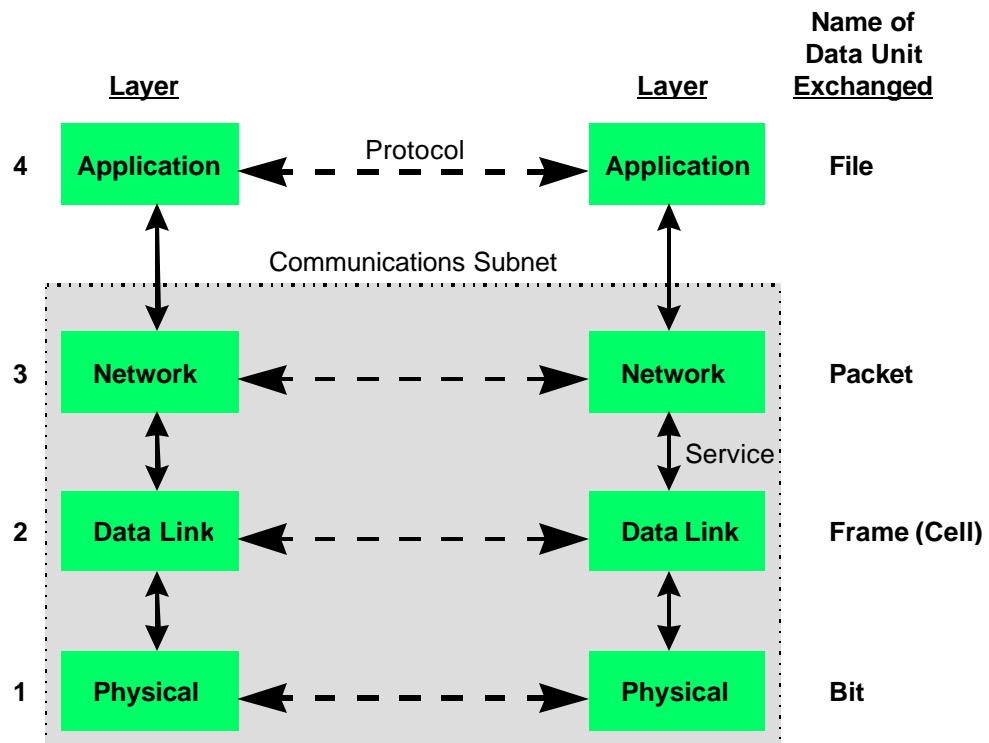
The interface to the WARP is via an intermediate assembly that converts RS-422 electrical levels to fiber optic signals. The specifics of the interface are described in the following sections.

### 1.5 Interface Layers Description

This document follows a modified Open Systems Interconnection (OSI) standard model that describes an interface between two systems. Each system performs functions that can be described as a series of layers. Each system has the same number of layers. The equivalent layers for each system have the same functions and communicate via an established protocol that is transparent to the protocols at the other layers. Each system passes data from its upper layers to its lower layers via a service provided by the next lower layer.

OSI uses seven layers to describe an interface; for this document four layers are used: the Physical Layer (Layer 1), the Data Link Layer (Layer 2), the Network Layer (Layer 3), and the Application

Layer (Layer 4). The first three layers are identical to those of the OSI standard and compose what is known as the communication subnet. The fourth layer corresponds to the upper, software-oriented functions of the interface in the OSI standard (Transport Layer, Session Layer, Presentation Layer, and Application Layer). Figure 1-1 illustrates the layer concept.



*Figure 1-1. OSI Layer Concept*

## Section 2. Physical Layer

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### 2.1 Function

The Physical Layer consists of two parts: the physical layer medium (the cabling and connectors, etc.) that makes up the physical connection between the two systems and the physical layer protocol that defines the lowest level of formatting (bit-level) of the data. The Physical Layer description is limited to those parts of the interface.

### 2.2 Mechanical Interface

#### 2.2.1 Envelope

The mechanical envelope of the WARP-to-AC interface is defined by an imaginary box that encases a 78-pin Subminiature D connector and its associated mating hardware [P/N 311407-5P-B-12](#).

#### 2.2.2 Coordinate System

The AC coordinates are defined in the EO-1 to LAC ICD, Section 3.

#### 2.2.3 Fasteners and Clamping

The fasteners and clamping for the AC/WARP interface shall be standard mating hardware for a 78-pin Subminiature D connector.

#### 2.2.4 Thermal Interface

There is no thermal requirement between the WARP and the AC.

### 2.3 Cable Type

#### 2.3.1 Maximum Cable Length

~~The interface to the WARP is through an intermediate assembly that converts the RS-422 differential signals to fiber optic signals.~~ The maximum cable length is 12 feet.

#### 2.3.2 Wire Gauge

The wires of the WARP/AC harness are ~~22-26~~ gauge.

#### 2.3.3 Shield Connections

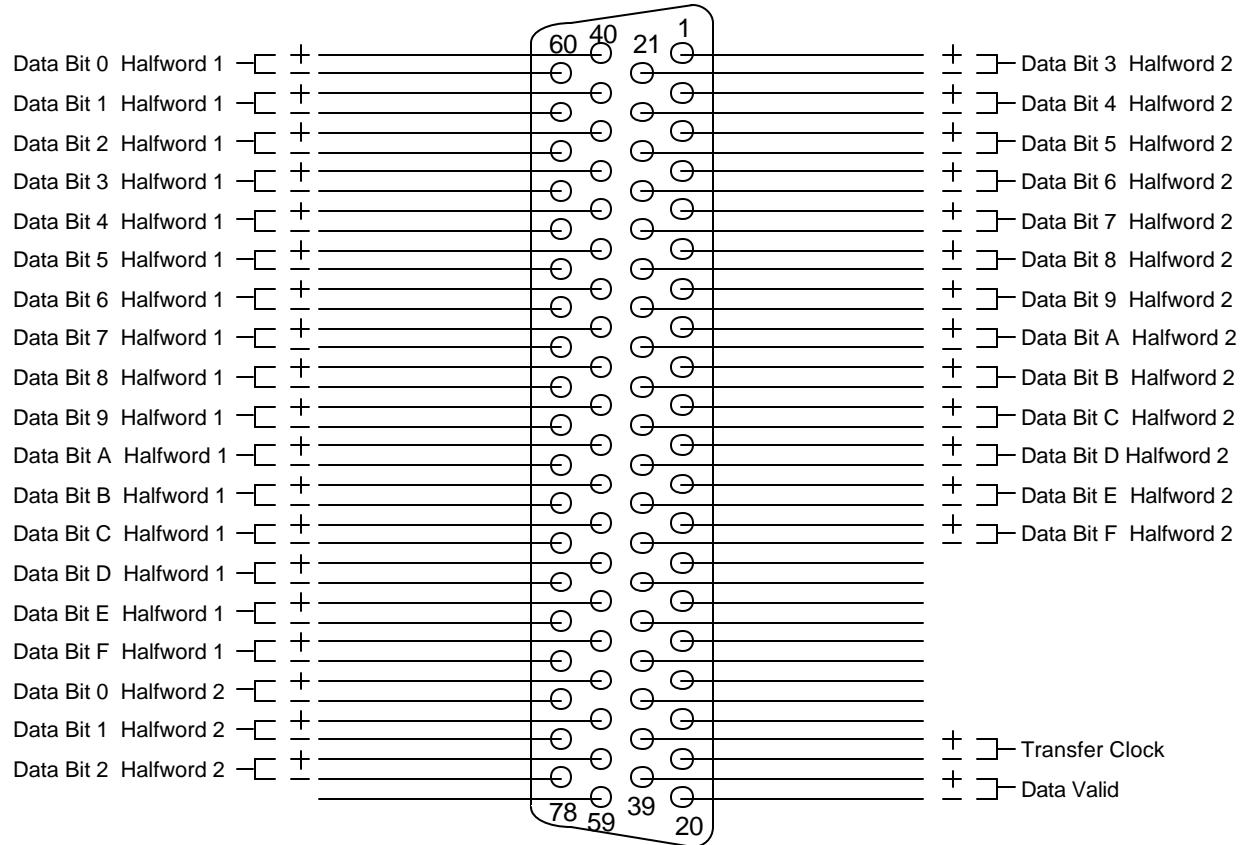
The shield connections of the AC/WARP harness shall conform to the System Level Electrical Requirements NMP EO-1 Flight, AM149-0020(155).

## 2.4 Connector Type

The WARP-to-AC interface consists of a 78-pin D Subminiature (DB-78) plug-type connector (Part Number M24308/8-349).

### 2.4.1 Connector Pin-Out

The connector pin-out is given in Figure 2-1.



**Figure 2-1. Connector (DB 78) Pin-Out**

### 2.4.2 AC-to-WARP Signal Mapping

The AC-to-WARP signal mapping is as follows:

Instrument Pin Name	WARP Pin Name	Pin Number
Data Bit F Halfword2_P	AC_DB31P	13
Data Bit F Halfword2_N	AC_DB31N	33
Data Bit E Halfword2_P	AC_DB30P	12
Data Bit E Halfword2_N	AC_DB30N	32
Data Bit D Halfword2_P	AC_DB29P	11

Instrument Pin Name	WARP Pin Name	Pin Number
Data Bit D Halfword2_N	AC_DB29N	31
Data Bit C Halfword2_P	AC_DB28P	10
Data Bit C Halfword2_N	AC_DB28N	30
Data Bit B Halfword2_P	AC_DB27P	9
Data Bit B Halfword2_N	AC_DB27N	29
Data Bit A Halfword2_P	AC_DB26P	8
Data Bit A Halfword2_N	AC_DB26N	28
Data Bit 9 Halfword2_P	AC_DB25P	7
Data Bit 9 Halfword2_N	AC_DB25N	27
Data Bit 8 Halfword2_P	AC_DB24P	6
Data Bit 8 Halfword2_N	AC_DB24N	26
Data Bit 7 Halfword2_P	AC_DB23P	5
Data Bit 7 Halfword2_N	AC_DB23N	25
Data Bit 6 Halfword2_P	AC_DB22P	4
Data Bit 6 Halfword2_N	AC_DB22N	24
Data Bit 5 Halfword2_P	AC_DB21P	3
Data Bit 5 Halfword2_N	AC_DB21N	23
Data Bit 4 Halfword2_P	AC_DB20P	2
Data Bit 4 Halfword2_N	AC_DB20N	22
Data Bit 3 Halfword2_P	AC_DB19P	1
Data Bit 3 Halfword2_N	AC_DB19N	21
Data Bit 2 Halfword2_P	AC_DB18P	58
Data Bit 2 Halfword2_N	AC_DB18N	78
Data Bit 1 Halfword2_P	AC_DB17P	57
Data Bit 1 Halfword2_N	AC_DB17N	77
Data Bit 0 Halfword2_P	AC_DB16P	56
Data Bit 0 Halfword2_N	AC_DB16N	76
Data Bit F Halfword1_P	AC_DB15P	55
Data Bit F Halfword1_N	AC_DB15N	75
Data Bit E Halfword1_P	AC_DB14P	54
Data Bit E Halfword1_N	AC_DB14N	74
Data Bit D Halfword1_P	AC_DB13P	53
Data Bit D Halfword1_N	AC_DB13N	73
Data Bit C Halfword1_P	AC_DB12P	52
Data Bit C Halfword1_N	AC_DB12N	72
Data Bit B Halfword1_P	AC_DB11P	51
Data Bit B Halfword1_N	AC_DB11N	71
Data Bit A Halfword1_P	AC_DB10P	50
Data Bit A Halfword1_N	AC_DB10N	70
Data Bit 9 Halfword1_P	AC_DB9P	49
Data Bit 9 Halfword1_N	AC_DB9N	69
Data Bit 8 Halfword1_P	AC_DB8P	48
Data Bit 8 Halfword1_N	AC_DB8N	68
Data Bit 7 Halfword1_P	AC_DB7P	47

Instrument Pin Name	WARP Pin Name	Pin Number
Data Bit 7 Halfword1_N	AC_DB7N	67
Data Bit 6 Halfword1_P	AC_DB6P	46
Data Bit 6 Halfword1_N		66
Data Bit 5 Halfword1_P	AC_DB5P	45
Data Bit 5 Halfword1_N	AC_DB5N	65
Data Bit 4 Halfword1_P	AC_DB4P	44
Data Bit 4 Halfword1_N	AC_DB4N	64
Data Bit 3 Halfword1_P	AC_DB3P	43
Data Bit 3 Halfword1_N	AC_DB3N	63
Data Bit 2 Halfword1_P	AC_DB2P	42
Data Bit 2 Halfword1_N	AC_DB2N	62
Data Bit 1 Halfword1_P	AC_DB1P	41
Data Bit 1 Halfword1_N	AC_DB1N	61
Data Bit 0 Halfword1_P	AC_DB0P	40
Data Bit 0 Halfword1_N	AC_DB0N	60
Transfer Clock_P	AC_CLKP	38
Transfer Clock_N	AC_CLKN	19
Data Valid_P	AC_VALIDP	39
Data Valid_N	AC_VALIDN	20

## 2.5 Bit-Level Timing

### 2.5.1 Rise Time

The rise time of the AC data lines is 1 ns minimum and ~~TBD-10~~ ns maximum.

### 2.5.2 Fall Time

The fall time of the AC data lines is 1 ns minimum and ~~TBD-10~~ ns maximum.

### 2.5.3 Clock Frequency

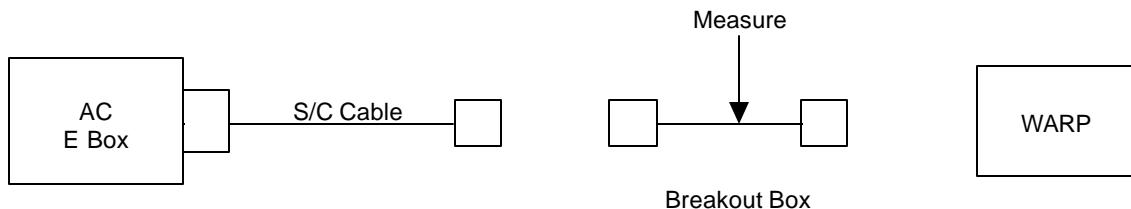
The data clock has two speeds: 6.0 MHz and 3.0 MHz. The data clock is set to the 6.0-MHz rate only during periods that the Advanced Land Imager (ALI) ~~and Hyperion are~~ is not on and the AC is set for a 60-Hz frame rate. The data clock is set for 3.0 MHz for all other frame rates. ~~For the slower frame rates (e.g., 2 Hz, 7.5 Hz, and 15 Hz), the data buffers may empty giving intraframe gaps in the data coming over the RS-422 link. During these gaps, the data valid bit will remain low~~

### 2.5.4 Data Valid

~~The Data Valid (DV) bit will transition from high to low when a 32-bit valid data word is on the bus and will remain low when data is not valid.~~

#### 2.5.4.1 Setup Time

The minimum setup time at room temperature for the 3-MHz frame rate shall be 50 ns. The minimum setup time at room temperature for the 6-MHz frame rate shall be 25 ns. All measurements shall be taken at the breakout box as shown in Figure 2-2.



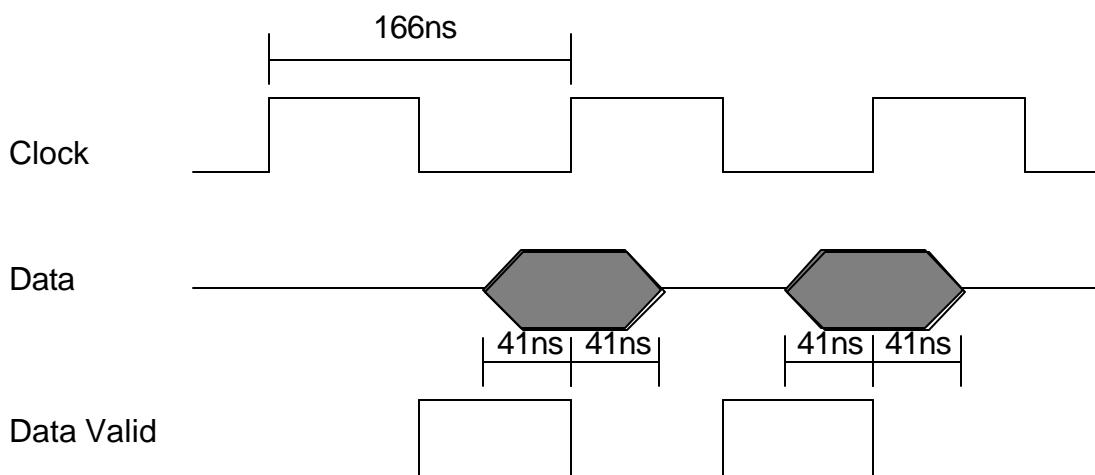
**Figure 2-2. TBS**

#### 2.5.4.2 Hold Time

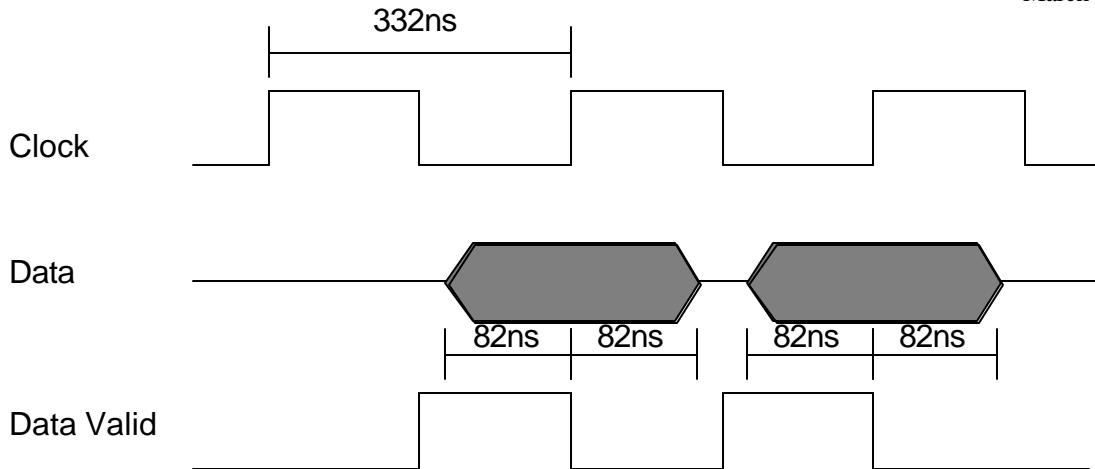
The minimum hold time at room temperature for the 3-MHz frame rate shall be 50 ns. The minimum hold time at room temperature for the 6-MHz frame rate shall be 40 ns. All measurements shall be taken at the breakout box as shown in Figure 2-2.

#### 2.5.45 Timing Diagrams

Figures 2-3 and 2-3-4 show the bit level timing for data transfers with respect to the data transfer clock and the data-valid signals. ~~The data valid bit is a gated clock, which is active only when data are on the bus. The data valid bit will transition~~ These timing diagrams refer to the output of the AC harness.



**Figure 2-32. Timing Diagram (6-MHz Transfer)**



**Figure 2-43. Timing Diagram (3-MHz Transfer)**

## 2.6 Signal Levels

### 2.6.1 Transmit Levels

The high-level output voltage of transmitted signals shall be greater than 2.5 V. The low-level output voltage measured across differential pairs shall be less than -2.5 V. Measurements will be taken at the breakout box as shown in Figure 2-2.

### 2.6.2 Deleted

## 2.7 Signal Grounding and Isolation

The signal grounding and isolation of the AC/WARP interface shall conform to the System Level Electrical Requirements NMP EP-1 Flight, AM149-0020(155).

## 2.8 Handling Procedures

The AC instrument hardware will be handled using standard ESD safeguards for space flight equipment.

## 2.9 EMI/EMC/RFI Specifications and Procedures

The AC-to-WARP RS-422 interface will comply with EO-1 Verification Plan and Environmental Specification, SAI-SPEC-158.

## Section 3. ~~Data Link Layer~~Deleted

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## Abbreviations and Acronyms

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$\mu$ sec	microsecond
AC	Atmospheric Corrector
ALI	Advanced Land Imager
<u>DV</u>	<u>data valid</u>
EMC	
EMI	
ESD	
Hz	hertz
ICD	interface control document
LAC	
LEISA	Linear Etalon Imaging Spectral Array
Mb	megabit
MHz	megahertz
ns	nanosecond
OSI	Open Systems Interconnection
RFI	radio frequency interference
V	volt
WARP	Wideband Advanced Recorder Processor